Group - 6

Topic: Experiment on Gate delays

Expression: $out = (\bar{a} \cdot \bar{b}) \cdot \bar{c}$

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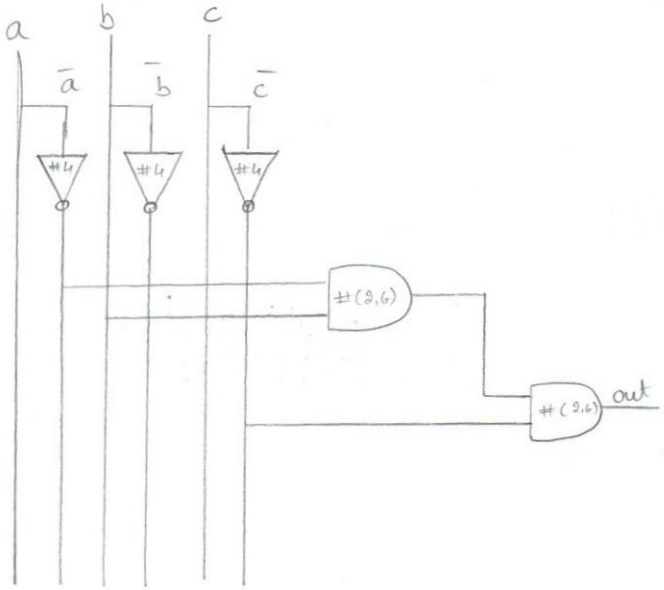
Bhumika SM - 1JB19EC019

1) Block diagram and Truthtable



a	b	c	ā	b̄	c̄	e = (ā·b̄)	out = (ā·b̄)c̄
0	0	0	1	1	1	1	1
0	0	1	1	1	0	1	0
0	1	0	1	0	1	0	0
0	1	1	1	0	0	0	0
1	0	0	0	1	1	0	0
1	0	1	0	1	0	0	0
1	1	0	0	0	1	0	0
1	1	1	0	0	0	0	0

2) VERILOG CODE

BHUMIKA S MURTHY
(1JB19EC019)

```
module group6 (out, a, b, c);
output out;
input a, b, c;
wire e, ab, bb, cb;
    not #(4) n1(ab,a);
    not #(4) n2(bb,b);
    not #(4) n3(cb,c);
    and #(2,6) a1(e, ab, bb);
    and #(2,6) a2(out, e, cb);
endmodule.
```

10/10

KEERTHANA. S.
(1JB19EC038)

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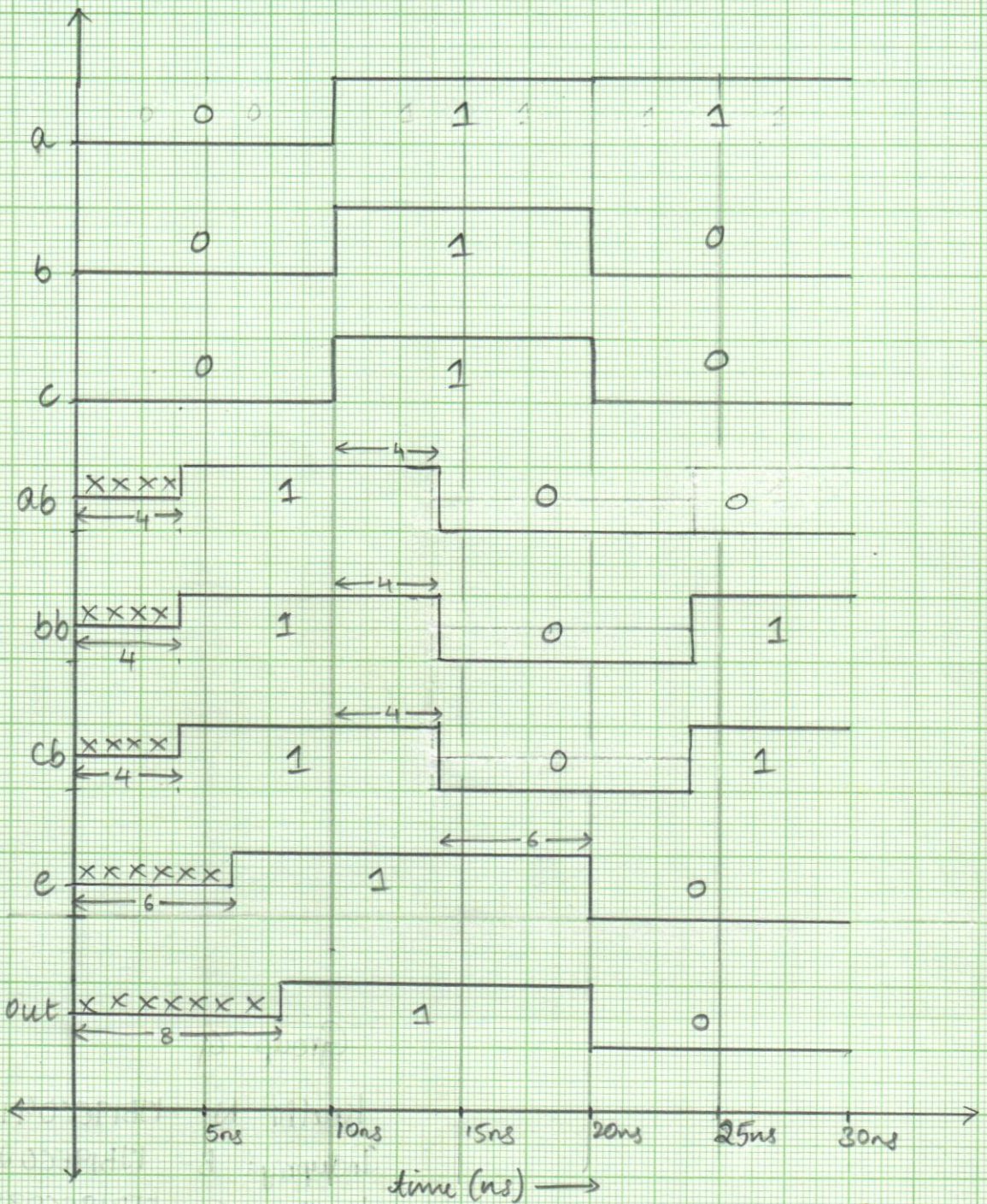
3.) VERILOG TESTBENCH

```
module test;
reg a, b, c;
wire out, e, ab, bb, cb;

group6 uut (.out(out), .a(a), .b(b), .c(c), .e(e), .ab(ab),
            .bb(bb), .cb(cb));

initial
begin
      a=0; b=0; c=0;
#10   a=1; b=1; c=1;
#10   a=1; b=0; c=0;
$monitor ($time, " Output = %b ", out);

end
endmodule
```

INDUPRIYA B
(1TB19EC029).

EXP. No.: Group 6 [5th sem 'A' sec] DATE : 08 12 2021



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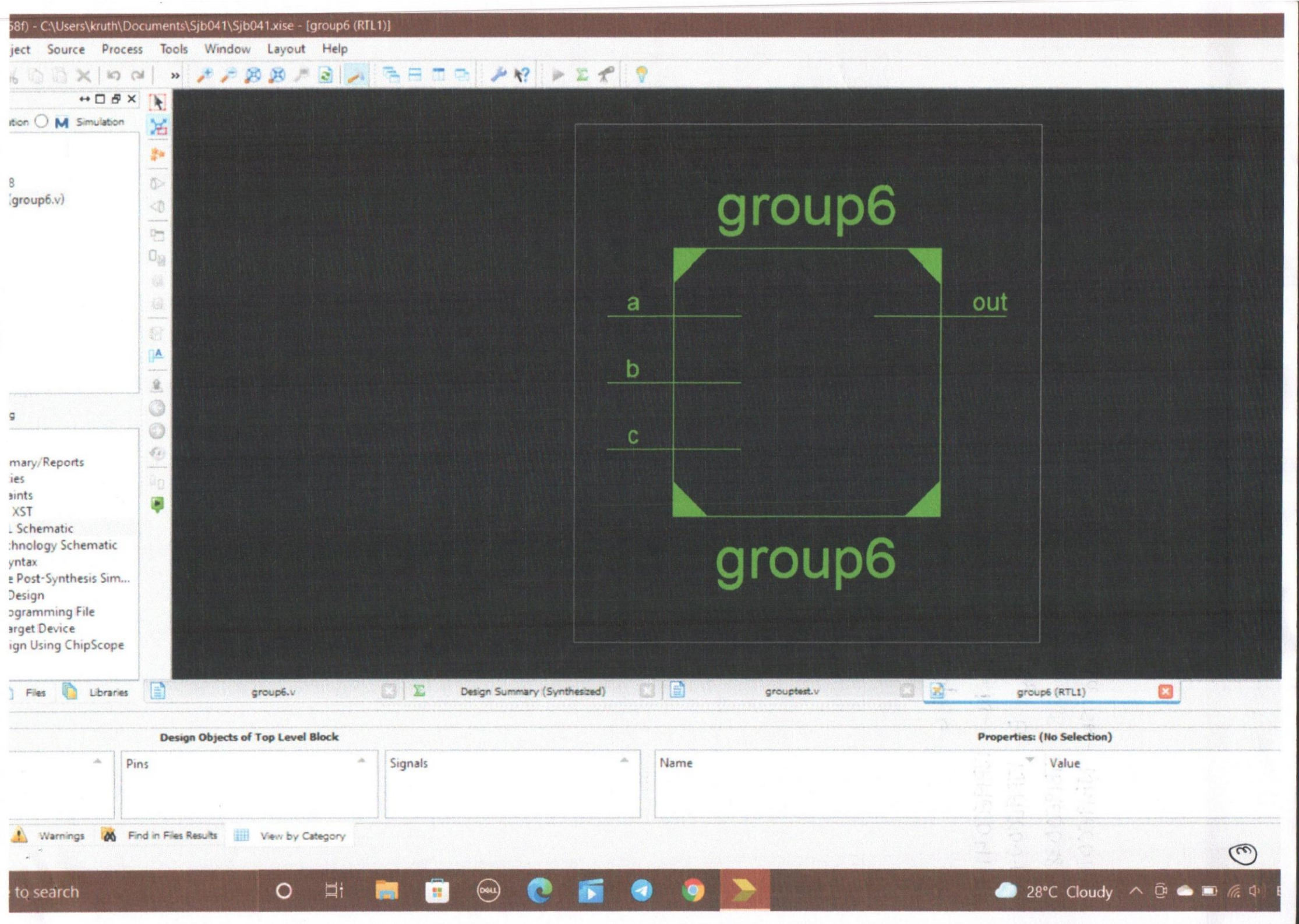
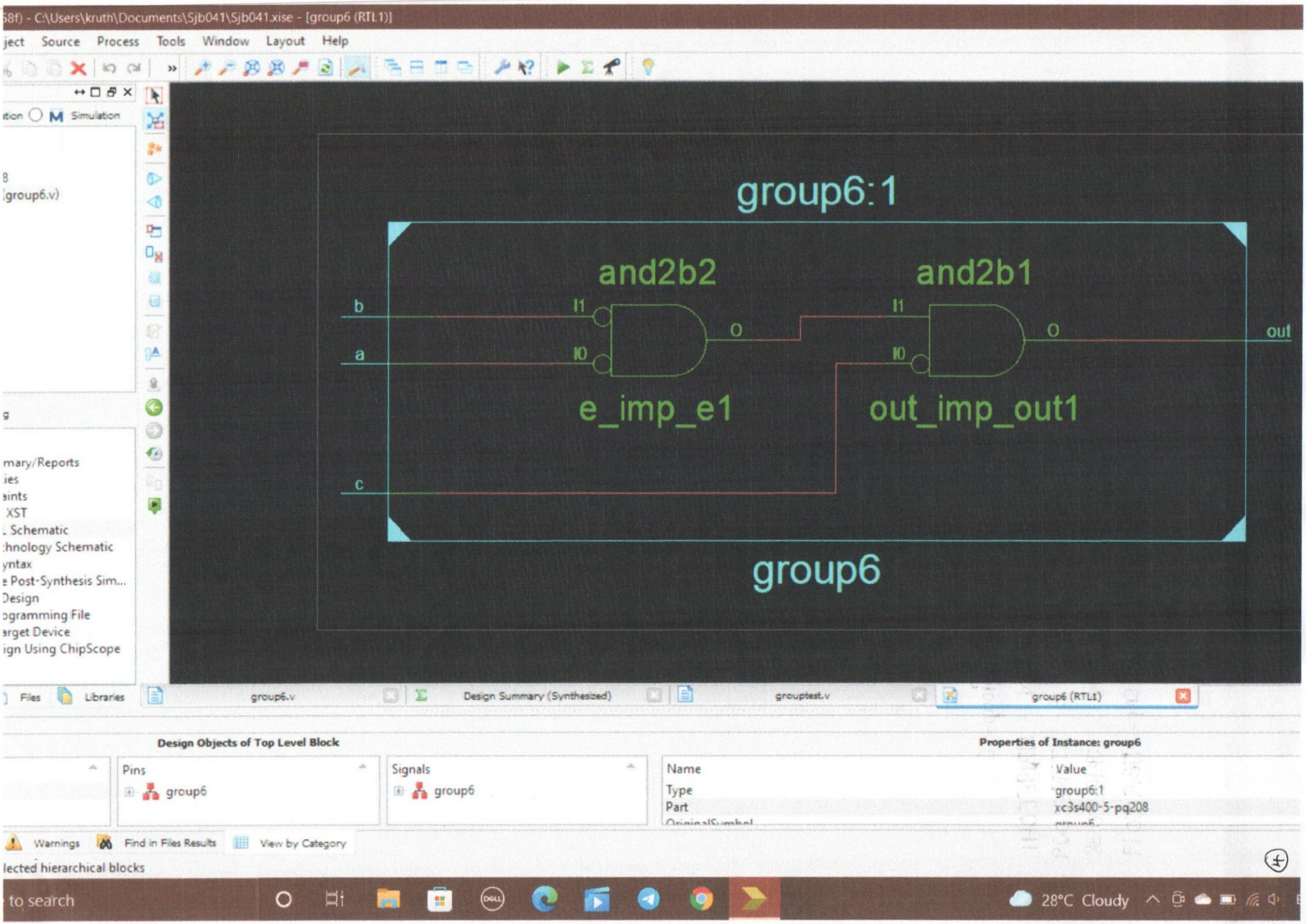

58f) - C:\Users\kruth\Documents\Sjb041\Sjb041.xise - [group6 (RTL1)]
ject Source Process Tools Window Layout Help
Simulation
(group6.v)
mary/Reports
ies
ints
XST
Schematic
hnology Schematic
yntax
Post-Synthesis Sim...
Design
ogramming File
arget Device
ign Using ChipScope
group6
a
b
c
out
group6
Files
Libraries
group6.v
Design Summary (Synthesized)
grouptest.v
group6 (RTL1)
Design Objects of Top Level Block
Properties: (No Selection)
Pins
Signals
Name
Value
Warnings
Find in Files Results
View by Category
to search
28°C Cloudy

Group - 6

Kruthi N - 1JB19EC041
Indupriya B - 1JB19EC029
Keerthna S - 1JB19EC038
Bhumika SM - 1JB19EC019.


C:\Users\kruth\Documents\Sjb041\Sjb041.xise - [group6 (RTL1)]
Source
Process
Tools
Window
Layout
Help
group6:1
and2b2
and2b1
b
a
c
I1
I0
O
I1
I0
O
out
e_imp_e1
out_imp_out1
group6
group6.v
Design Summary (Synthesized)
grouptest.v
group6 (RTL1)
Design Objects of Top Level Block
Pins
group6
Signals
group6
Properties of Instance: group6
Name
Value
Type
group6:1
Part
xc3s400-5-pq208
Warnings
Find in Files Results
View by Category
28°C Cloudy

Group - 6
Kruthi. N - 1JB19EC041
Indupriya B - 1JB19EC029
Keerthna S - 1JB19EC038
Bhumika SM - 1JB19EC019

58f) - C:\Users\kruth\Documents\Sjb041\Sjb041.xise - [group6.v]

ject Source Process Tools Window Layout Help

```
1  `timescale 1ns / 1ps
2  //////////////////////////////////////////////////////////////////////////////////
3  // Company:
4  // Engineer:
5  //
6  // Create Date:    15:27:20 12/07/2021
7  // Design Name:
8  // Module Name:    group6
9  // Project Name:
10 // Target Devices:
11 // Tool versions:
12 // Description:
13 //
14 // Dependencies:
15 //
16 // Revision:
17 // Revision 0.01 - File Created
18 // Additional Comments:
19 //
20 //////////////////////////////////////////////////////////////////////////////////
21 module group6(out,a,b,c);
22 output out;
23 input a,b, c;
24 wire e, ab,bb,cb;
25    not #(4) n1(ab,a);
26    not #(4) n2(bb,b);
27    not #(4) n3(cb,c);
28    and #(2,6) a1(e,ab,bb);
29    and #(2,6) a2(out,e,cb);
30 endmodule
31
```

Simulation

grouptest.v)

imulator
Behavioral Model

Files Libraries

group6.v Design Summary grouptest.v

dialog select the ModelSim executable that you wish to use
Then try this Process again.

Warnings Find in Files Results

to search

28°C Cloudy

Group-6

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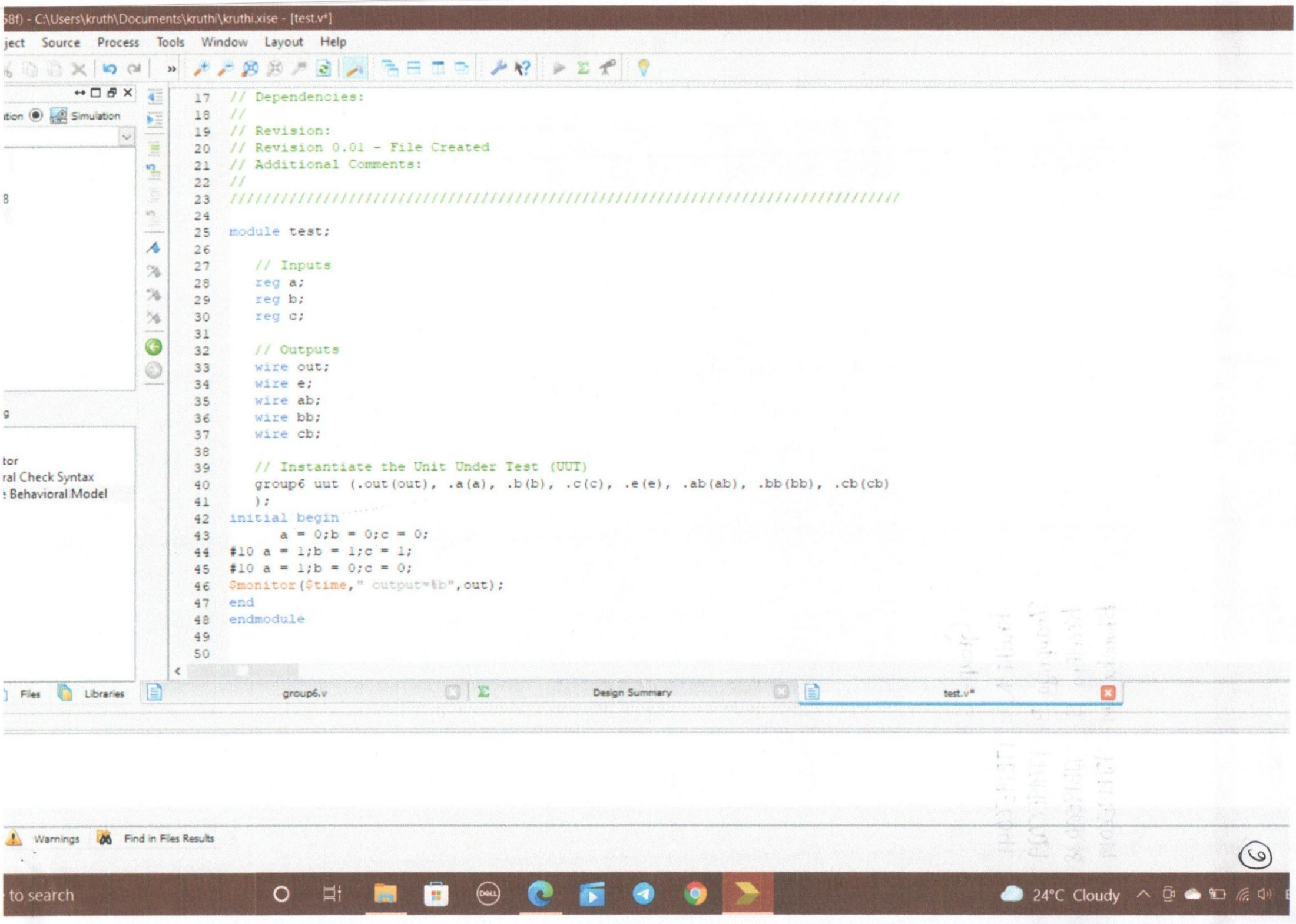
58f) - C:\Users\kruth\Documents\kruthi\kruthi.xise - [test.v*]
ject Source Process Tools Window Layout Help
17 // Dependencies:
18 //
19 // Revision:
20 // Revision 0.01 - File Created
21 // Additional Comments:
22 //
23 //
24
25 module test;
26
27 // Inputs
28 reg a;
29 reg b;
30 reg c;
31
32 // Outputs
33 wire out;
34 wire e;
35 wire ab;
36 wire bb;
37 wire cb;
38
39 // Instantiate the Unit Under Test (UUT)
40 group6 uut (.out(out), .a(a), .b(b), .c(c), .e(e), .ab(ab), .bb(bb), .cb(cb)
41);
42 initial begin
43 a = 0;b = 0;c = 0;
44 #10 a = 1;b = 1;c = 1;
45 #10 a = 1;b = 0;c = 0;
46 $monitor($time," output=%b",out);
47 end
48 endmodule
49
50
Simulation
tor
ral Check Syntax
Behavioral Model
Files
Libraries
group6.v
Design Summary
test.v*
Warnings
Find in Files Results
to search
24°C Cloudy

Group- 6

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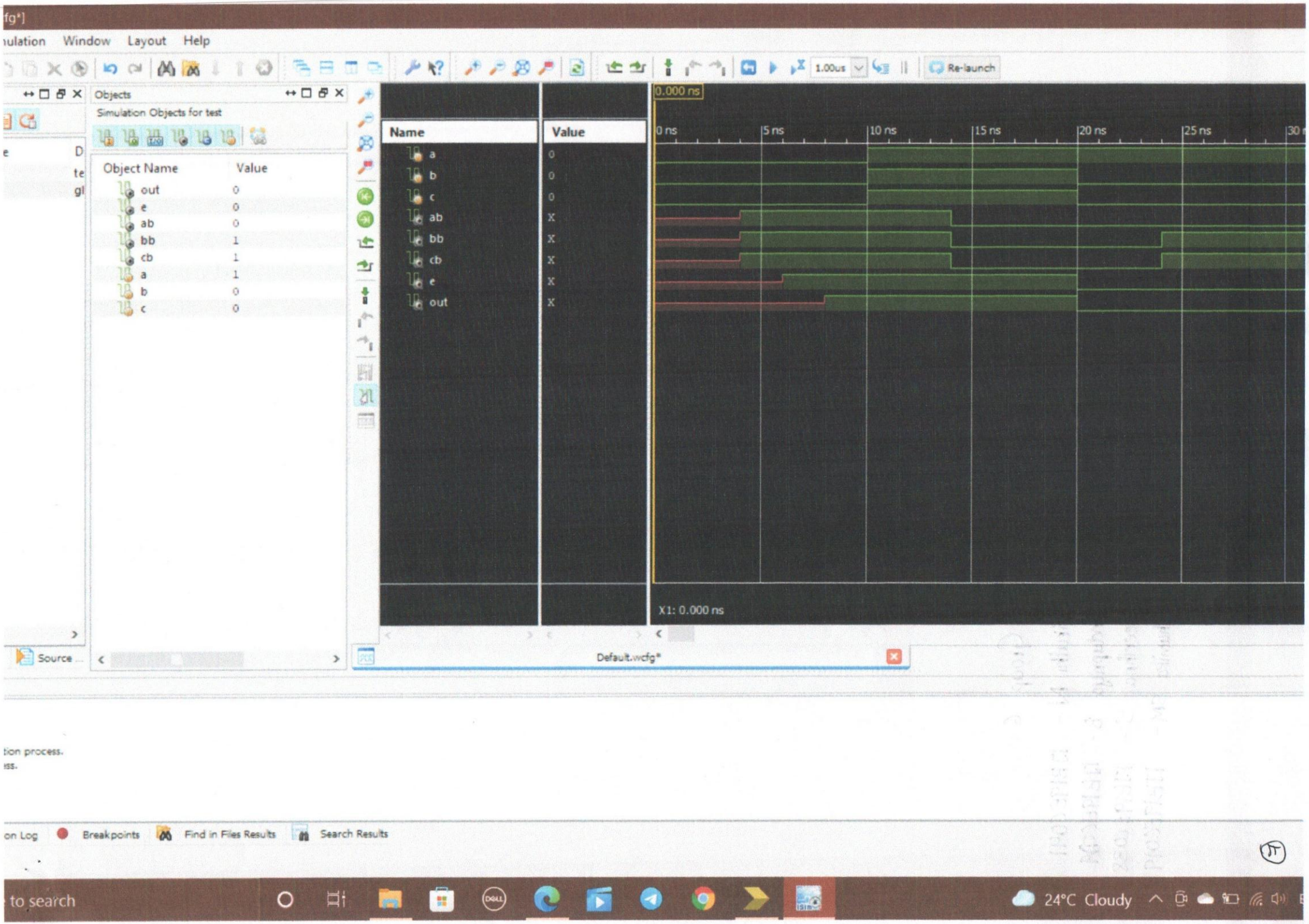
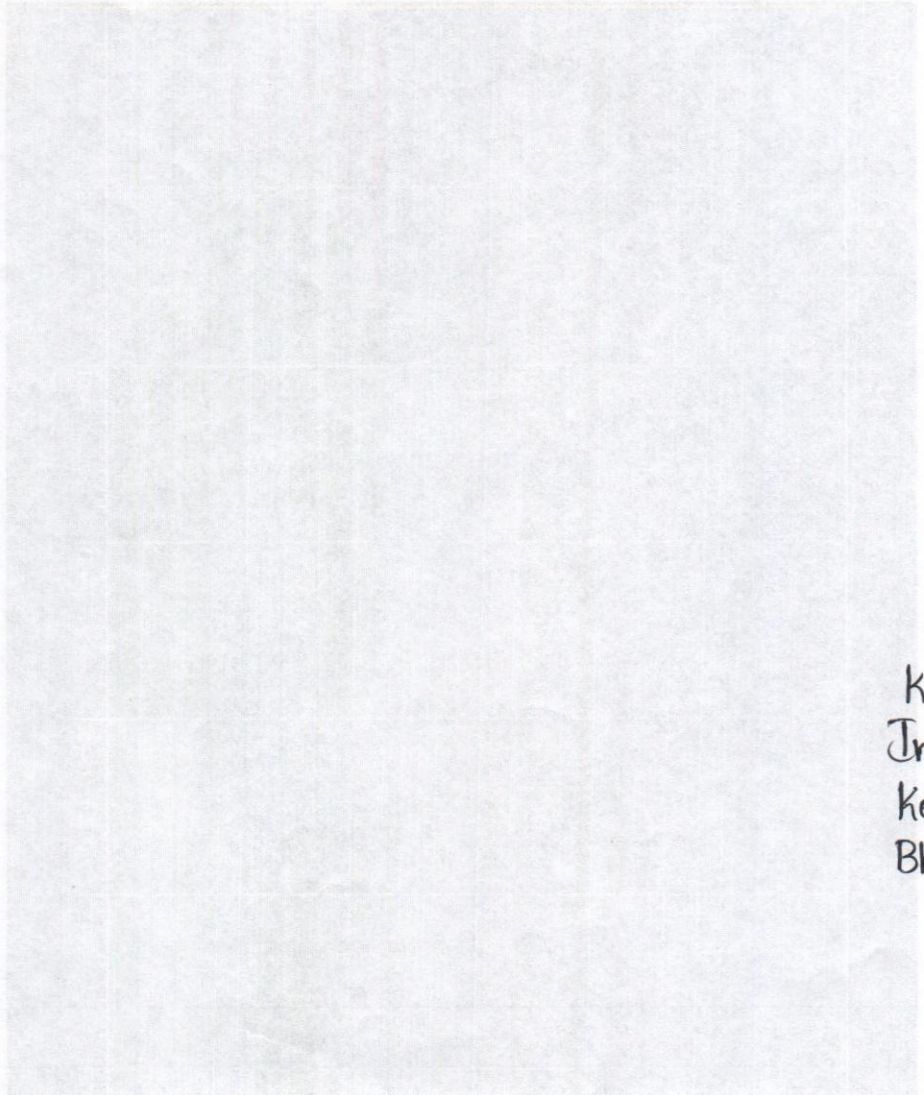

fg*]
ulation Window Layout Help
Re-launch
Objects
Simulation Objects for test
Object Name Value
out 0
e 0
ab 0
bb 1
cb 1
a 1
b 0
c 0
Name Value
a 0
b 0
c 0
ab X
bb X
cb X
e X
out X
0.000 ns
0 ns 5 ns 10 ns 15 ns 20 ns 25 ns
X1: 0.000 ns
Source ...
Default.wcfg*
Breakpoints
Find in Files Results
Search Results
to search
24°C Cloudy



Group - 6

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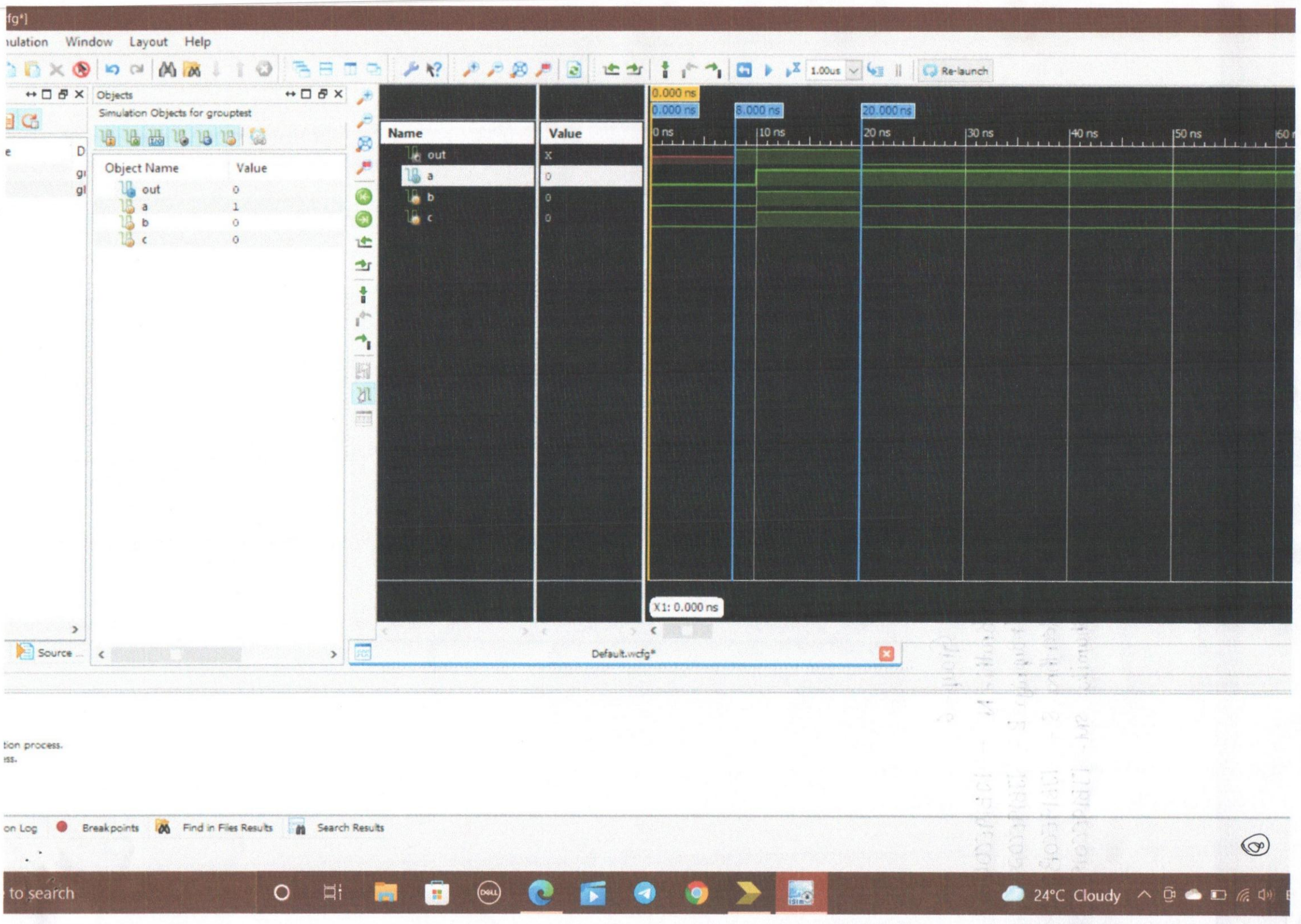
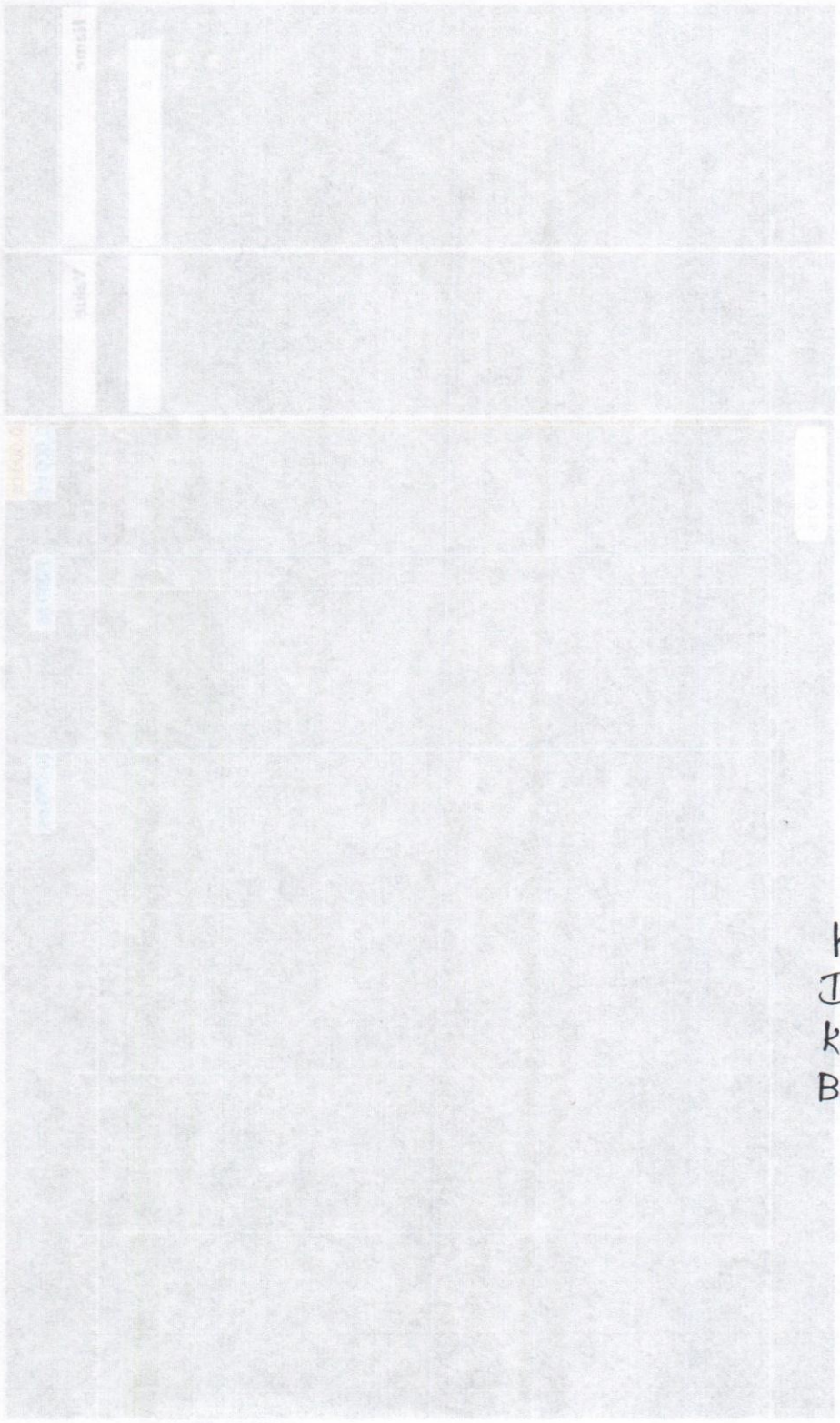
Bhumika SM - 1JB19EC019


fg*]
ulation Window Layout Help
Re-launch
1.00us
Objects
Simulation Objects for grouptest
Object Name Value
out 0
a 1
b 0
c 0
Name Value
out X
a 0
b 0
c 0
0.000 ns
0.000 ns
5.000 ns
20.000 ns
0 ns 10 ns 20 ns 30 ns 40 ns 50 ns
X1: 0.000 ns
Source ...
Default.wcfg*
tion process.
iss.
on Log Breakpoints Find in Files Results Search Results
to search
24°C Cloudy



Group - 6

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Indupriya B – 1JB19EC029

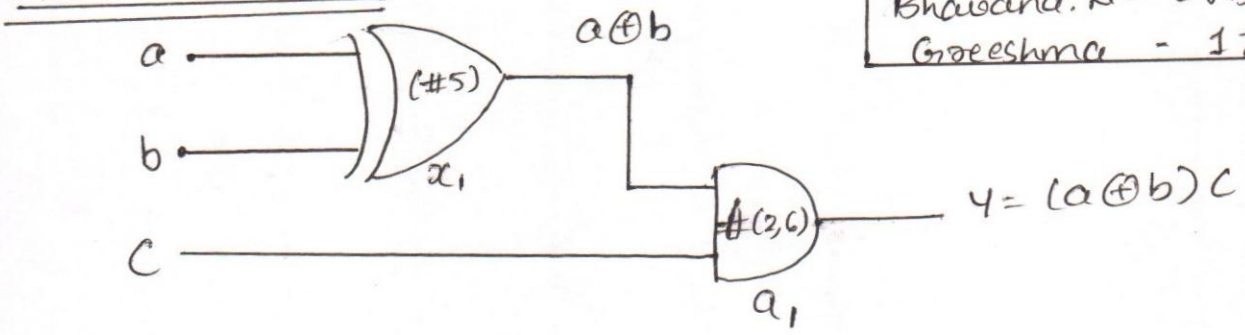
Keerthna S – 1JB19EC038

Bhumika SM – 1JB19EC019

Group No - G2
Kavana.T.R - 1JB20EC409
Lavanya.B.P. - 1JB19EC044
Bhavana.N - 1JB19EC015
Greeshma - 1JB19EC046

Expression ⇒ $Y = (a \oplus b)C$

Circuit diagram



Truth table

A	b	x	C	Y
0	0	0	0	0
0	1	1	0	0
1	0	1	1	1
1	1	0	1	0

Kavana.T.R.
1JB20EC409

10/10

Head
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Program

```
module gatedelay(a,b,c,y)
 input a,b,c;
 output y;
 wire x;
 xor #(5) x1(x,a,b);
 and #(2,6) a1(y,x,c);
 endmodule
```

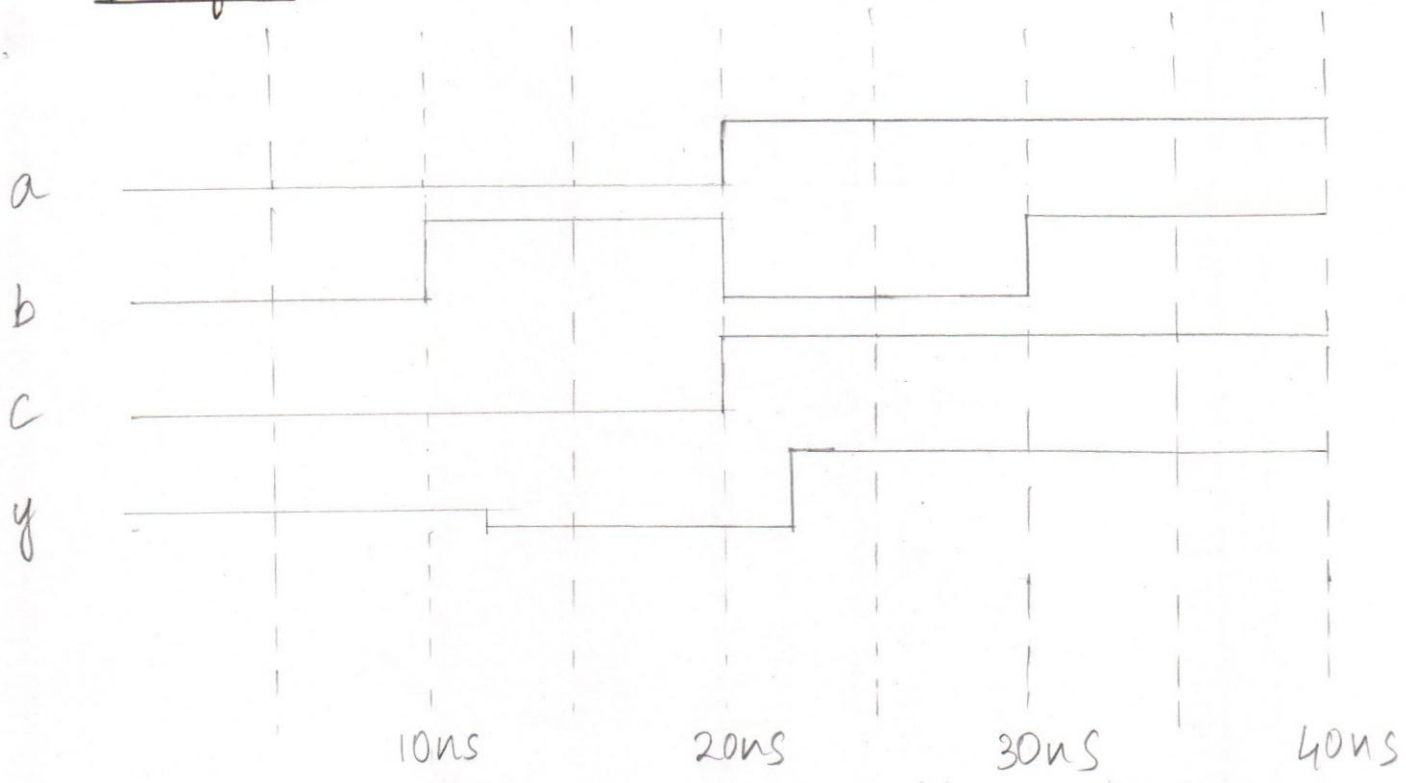
Lavanya. B.P.
1JB19EC044

Testbench

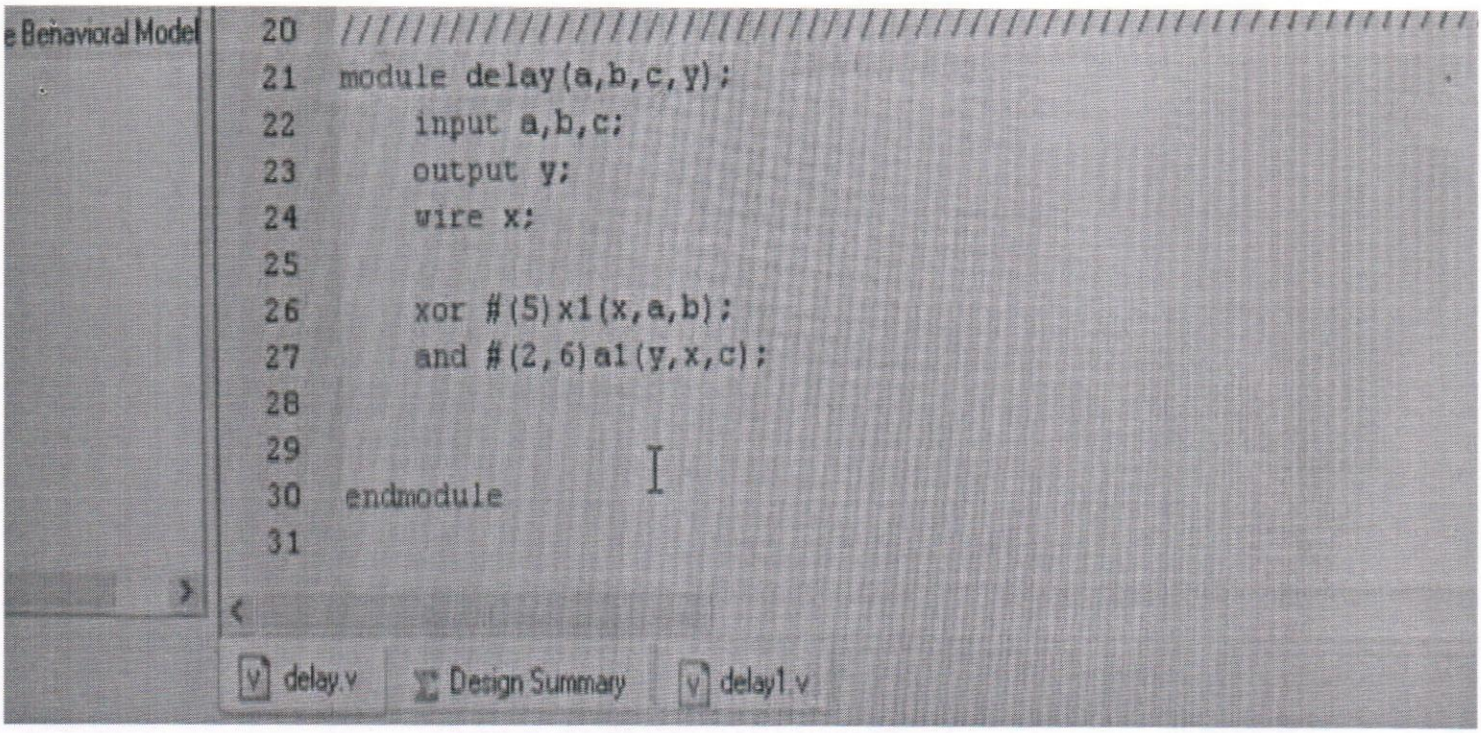
```
module test;
 reg a,b,c;
 wire y;
 gatedelay g1(a,b,c,y);
 initial
 begin
 a=0; b=0; c=0;
#10 a=0; b=1; c=0;
#10 a=0; b=1; c=0;
#10 a=1; b=0; c=1;
#10 a=1; b=1; c=1;
#10 $finish;
 end
 endmodule
```

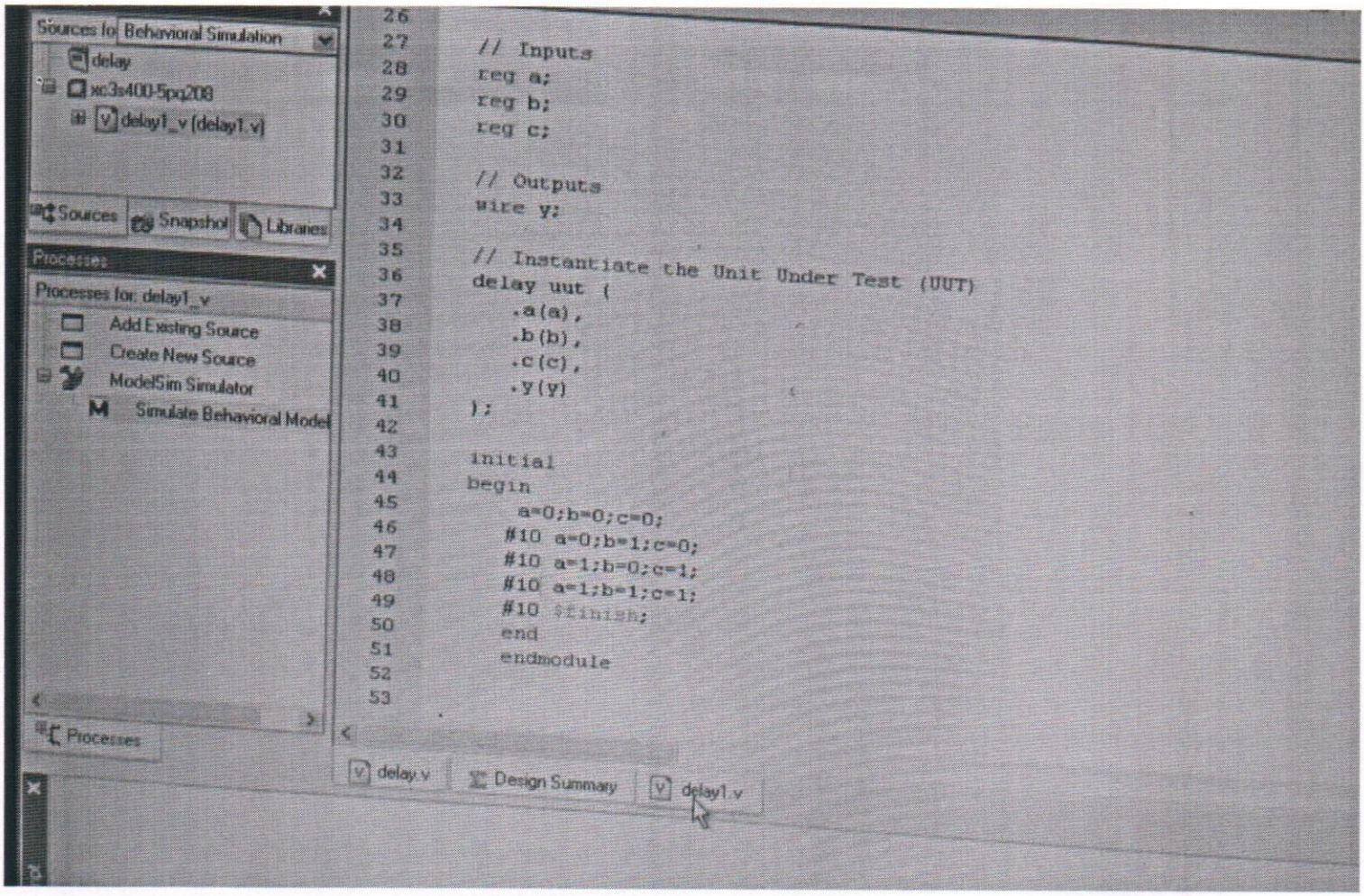
Bhavana
1JB19EC015

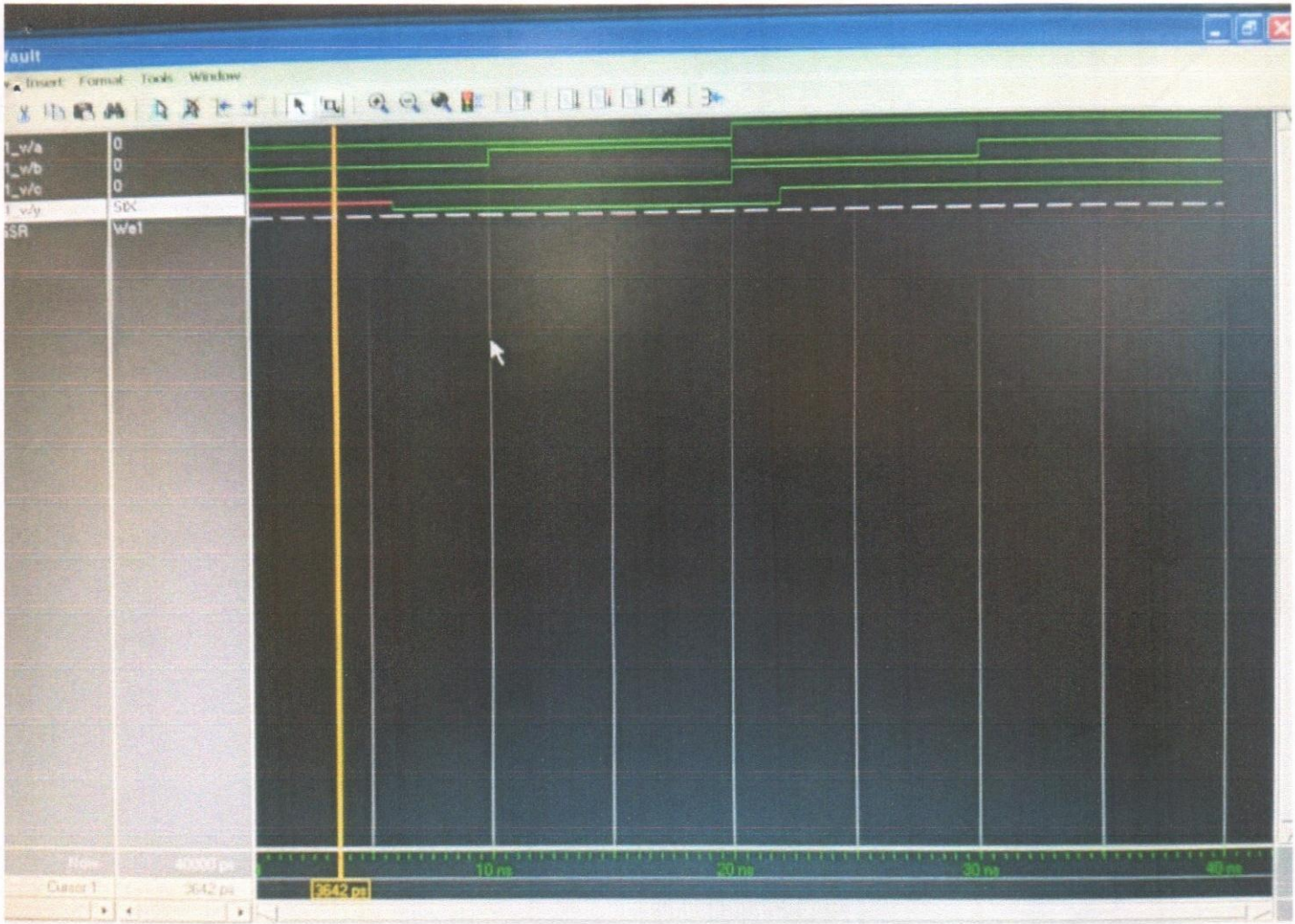
Waveform:-



M.S. GREESHMA CHOWDHARY
1JB19EC046


e Behavioral Model
20 //
21 module delay(a,b,c,y);
22 input a,b,c;
23 output y;
24 wire x;
25
26 xor #(5)x1(x,a,b);
27 and #(2,6)a1(y,x,c);
28
29
30 endmodule
31
delay.v
Design Summary
delay1.v


Sources for: Behavioral Simulation
delay
xc3s400-5pq208
delay1_v (delay1.v)
Sources
Snapshot
Libraries
Processes
Processes for: delay1_v
Add Existing Source
Create New Source
ModelSim Simulator
Simulate Behavioral Model
Processes
26
27 // Inputs
28 reg a;
29 reg b;
30 reg c;
31
32 // Outputs
33 wire y;
34
35 // Instantiate the Unit Under Test (UUT)
36 delay uut (
37 .a(a),
38 .b(b),
39 .c(c),
40 .y(y)
41);
42
43 initial
44 begin
45 a=0;b=0;c=0;
46 #10 a=0;b=1;c=0;
47 #10 a=1;b=0;c=1;
48 #10 a=1;b=1;c=1;
49 #10 $finish;
50 end
51 endmodule
52
53
delay.v
Design Summary
delay1.v


Insert Format Tools Window
1_w/a
1_w/b
1_w/c
1_w/y
SR
0
0
0
SIX
Wel
Now
Cursor 1
3642 ps
10 ns
20 ns
30 ns
40 ns