



||Jai Sri Gurudev||

Sri AdichunchanagiriShikshana Trust (R)  
SJB INSTITUTE OF TECHNOLOGY

(Affiliated to Visvesvaraya Technological University, Belagavi & Approved by AICTE, New Delhi)

No. 67, BGS Health & Education City, Dr. Vishnuvardhan Road, Kengeri, Bengaluru-560060.

DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING



Subject: Verilog HDL

Faculty Name	Designation	Sem & Sec	Topic	Date	Time
Mrs. Latha S	Assistant Professor	5 <sup>th</sup> A	Gate level modelling	23/12/2021	02.30 pm – 03.30 pm

PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
✓	✓											✓		

*Latha*  
Faculty Signature

*[Signature]*  
Head

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||Jai Sri Gurudev||

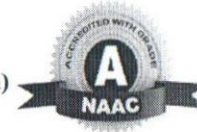
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**Subject: Verilog HDL 18EC56**

Faculty Name	Designation	Sem & Sec	Topic	Date	Time
Mrs. Latha S	Assistant Professor	5 <sup>th</sup> A	Verilog HDL:A solution for Everybody	25/11/2021	02.30 pm – 03.30 pm

PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
✓	✓											✓		

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