||Jai Sri Gurudev||
Sri Adichunchanagiri Shikshana Trust (R)
**SJB INSTITUTE OF TECHNOLOGY**
(Affiliated to Visvesvaraya Technological University, Belagavi & Approved by AICTE, New Delhi)
No. 67, BGS Health & Education City, Dr. Vishnuvardhan Road, Kengeri, Bengaluru-560060.

DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

# Module Wise Plan

| Course Title: Verilog HDL | | | Course Code: 18EC56 |
|---|---|---|---|
| Semester: V 'A' | Academic Year: 2021-22 | Total hrs.: 40 | Hrs./Week: 03 |
| Int. Exam Hrs.: 01 | Internal Evaluation Max. Marks: 40 | | |
| Ext. Exam Hrs.: 03 | Ext. Exam Max.Marks: 60 | | |
| Lesson Plan Author / Desgn. / Dept.: LATHA S / Assistant Professor/ ECE | | | |

## Course Objectives:

This course will enable students to:

- Designing digital circuits, behavioral and RTL modeling of digital circuits using Verilog HDL.
- Verifying these models and synthesizing RTL models to standard cell libraries and FPGAs
- Provide better understanding of the different technologies related to HDLs, construct, compile and execute Verilog HDL programs using provided software tools.
- Design digital components and circuits that are testable, reusable and synthesizable.

## Course Outcomes:

After studying this course, students will be able to:

- Understand the usage of Verilog Hardware Description Language (HDL) in Semiconductor Technology and Design flow of Digital Circuits.
- Interpret the various constructs in logic synthesis and perform timing and delay Simulation
- Design and verify the functionality of digital circuit/system using test benches.
- Develop Verilog programs in gate, dataflow (RTL), behavioural and switch modelling levels of Abstraction.
- Analyze the programs more effectively using Verilog tasks, functions and directives.

| DAYS | Module No. & Title | SUBTOPICS | CO |
|---|---|---|---|
| 1 | **Module 1: Overview of Digital Design with Verilog HDL & Hierarchical Modeling Concepts** | Evolution of CAD | CO1 |
| 2 | | Emergence of HDLs, Typical HDL-flow | CO1 |
| 3 | | Why Verilog HDL? trends in HDLs | CO1 |
| 4 | | Top-down design methodology | CO1 |
| 5 | | Bottom-up design methodology | CO1 |
| 6 | | Examples for top-down designing | CO1 |
| 7 | | Differences between modules and module instances | CO2 |

| | | | |
|---|---|---|---|
| 8 | | Simulation - design block, stimulus block | CO2 |
| 9 | **Module 2: Basic Concepts & Modules and Ports** | Basic Concepts – Introduction to Structure | CO3 |
| 10 | | Lexical conventions | CO3 |
| 11 | | Data types, System tasks | CO3 |
| 12 | | Compiler directives | CO3 |
| 13 | | Module definition | CO3 |
| 14 | | Port declaration | CO3 |
| 15 | | Connecting ports | CO3 |
| 16 | | Hierarchical name referencing | CO3 |
| 17 | **Module 3: Gate-Level & Dataflow Modeling** | Basic Verilog gate primitives | CO4 |
| 18 | | Description of and/or and buf /not type gates | CO4 |
| 19 | | Rise, fall and turn-off delays | CO4 |
| 20 | | Min, max, and typical delays | CO4 |
| 21 | | Continuous assignments | CO4 |
| 22 | | Delay specification | CO4 |
| 23 | | Expressions, Operators, operands | CO4 |
| 24 | | Operator types | CO4 |
| 25 | **Module 4: Behavioral Modeling, Tasks and Functions:** | Structured procedures, Initial and always | CO4 |
| 26 | | Blocking and non-blocking statements | CO4 |
| 27 | | Delay control, Generate statement | CO4 |
| 28 | | Event control, Conditional statements | CO4 |
| 29 | | Multiway branching, loops | CO4 |
| 30 | | Sequential blocks, parallel blocks. | CO4 |
| 31 | | Differences between tasks and functions | CO5 |
| 32 | | Declaration, invocation, automatic tasks and functions | CO5 |
| 33 | **Module 5: Useful Modeling Techniques & Logic Synthesis with Verilog** | Procedural continuous assignments | CO5 |
| 34 | | overriding parameters, | CO5 |
| 35 | | conditional compilation and execution | CO5 |
| 36 | | useful system tasks | CO5 |
| 37 | | Logic Synthesis | CO2 |
| 38 | | Impact of logic synthesis | CO2 |
| 39 | | Verilog HDL Synthesis | CO2 |
| 40 | | Synthesis design flow, Verification of Gate-Level netlist | CO2 |

# Reference / Textbook Details

| Sl.No. | Title of Book | Author | Publication | Edition |
|---|---|---|---|---|
| 1 | Verilog HDL: A Guide to Digital Design and Synthesis | Samir Palnitkar | Pearson Education | 2nd |
| 2 | VHDL for Programmable Logic | Kevin Skahill | PHI/Pearson education | 2nd |
| 3 | The Verilog Hardware Description Language | Donald E. Thomas, Philip R. Moorby | Springer Science+Business Media, LLC | 5th |
| 4 | Advanced Digital Design with the Verilog HDL | Michael D. Ciletti | Pearson (Prentice Hall) | 2nd |
| 5 | Design through Verilog HDL | Padmanabhan, Tripura Sundari | Wiley | Latest |

**[LATHA S]**
**Faculty In-Charge**
**Date:**

**Head of the Department**

Dept. of Electronics & Communication Engg.
SJB Institute of Technology
Bengaluru-560060